Aninda Manocha

Computer Science PhD Student | Princeton University

@ amanocha@princeton.edu
35 Olden Street, Princeton, NJ 08540
http://www.cs.princeton.edu/ amanocha/
linkedin.com/in/anindamanocha github.com/amanocha

I am a fifth-year graduate student in Computer Science at Princeton University with a focus on Computer Architecture. My dissertation work aims to optimize the mapping of irregular applications with sparse, memory-bound characteristics onto modern hardware. I work within the context of the DECADES project, which has resulted in a chip tapeout to demonstrate the promise of a heterogeneous tile-based architecture designed for several emerging workflows in the broad areas of machine learning and graph analytics. Emphasizing hardware-software co-design approaches, I have developed compiler and architecture techniques to improve the performance, power efficiency, and programmability of such applications. I have also designed memory hierarchy approaches tailored to address memory latency and bandwidth bottlenecks. Currently, my work focuses on hardware and operating system techniques to more efficiently manage huge pages for irregular applications.

Education

Exp. May 2023 – August 2018 | **Princeton University**, Princeton, New Jersey
- Ph.D. Computer Science
- Advisor: Prof. Margaret Martonosi

May 2020 – August 2018 | **Princeton University**, Princeton, New Jersey
- M.A. Computer Science

May 2018 – August 2015 | **Duke University**, Durham, North Carolina
- B.S. Electrical and Computer Engineering, Computer Science, *Cum Laude*

June 2015 – August 2013 | **The North Carolina School of Science and Mathematics**, Durham, North Carolina
- High School Diploma

Research Experience

Present – August 2018 | **Research Assistant**, Princeton University Department of Computer Science
Advisor: Prof. Margaret Martonosi
- Developing hardware-software co-design and memory hierarchy approaches to target irregular memory access bottlenecks in graph and sparse applications
- Designing reconfigurable optimizations to support applications whose characterizations range from dense and compute-intensive to sparse and memory-intensive
- Contributing to the development of a specialized, reconfigurable hardware platform for accelerating different software applications on the fly as part of DARPA's Software Defined Hardware (SDH) program

June 2018 – August 2017 | **Research Assistant**, Duke University Department of Electrical and Computer Engineering
Advisor: Prof. Benjamin C. Lee
- Studied Bayesian optimization and other statistical machine learning methods to jointly optimize parameters for high-level synthesis (HLS)
- Created a framework that runs the optimization to configure directives and quickly discovers Pareto optimal design points
- Outperformed other optimization algorithms in efficiency, such as simulated annealing, genetic algorithm, and random search

May 2017 – January 2017 | **Research Assistant**, Duke University Department of Electrical and Computer Engineering
Advisor: Prof. Benjamin C. Lee
- Evaluated an Android-based crowd computing framework and brought it up to date
- Deployed framework on different systems (emulator, phone, and tablet) using an OpenCV facial recognition application
- Modified framework to run a small and simple application and grow familiar with its topology

June 2015 – August 2014 | **Research Assistant, Duke University Department of Mathematics**
Advisors: Prof. Lenhard Ng (Duke University) and Dr. Daniel J. Teague (NCSSM)

- Studied Knot Theory and the different types representations of knots
- Focused on properties of Legendrian knots to classify other knots and extend an existing knot atlas
- Developed a Java program to identify isotopic Legendrian knots and enumerate transverse knots

December 2014 – March 2014 | **Research Assistant, University of North Carolina at Chapel Hill Department of Applied Mathematics**
Advisor: Prof. Gregory Forest

- Studied viruses in the human lung to explore gene therapy as a means of treating cystic fibrosis (CF)
- Extended a computational model of virus motion in the respiratory system of a CF patient
- Experimented with various physiological parameters to shed light on additions to gene therapy for CF

Publications

- **Aninda Manocha**, Zi Yan, Esin Tureci, Juan Luis Aragón, David Nellans, and Margaret Martonosi. "The Implications of Page Size Management on Graph Analytics." In *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*. IEEE 2022.
- Marcelo Orenes Vera, **Aninda Manocha**, Jonathan Balkind, Fei Gao, Juan Luis Aragón, David Wentzlaff, and Margaret Martonosi. "Tiny but Mighty: Designing and Realizing Scalable Latency Tolerance for Manycore SoCs." In *Proceedings of the International Symposium on Computer Architecture (ISCA)*. ACM 2022.
- **Aninda Manocha**, Juan Luis Aragón, and Margaret Martonosi. "Graphfire: Synergizing Fetch, Insertion, and Replacement Policies for Graph Analytics." In *IEEE Transactions on Computers*. IEEE Press 2022.
- Marcelo Orenes Vera, **Aninda Manocha**, David Wentzlaff, and Margaret Martonosi. "AutoSVA: Democratizing Formal Verification of RTL Module Interactions." In *The Design Automation Conference (DAC)*. IEEE Press, 2021.
- **Aninda Manocha**, Tyler Sorensen, Esin Tureci, Opeoluwa Matthews, Juan Luis Aragón, and Margaret Martonosi. "GraphAttack: Optimizing Data Supply for Graph Applications on In-Order Multicore Architectures." In *ACM Transactions on Architecture and Code Optimization (TACO)*. ACM 2021.
- Tyler Sorensen, **Aninda Manocha**, Marcelo Orenes-Vera, Esin Tureci, Juan L. Aragon, and Margaret Martonosi. "A Simulator and Compiler Framework for Agile Hardware-Software Co-design Evaluation and Exploration." Invited Talk in *The IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. IEEE Press, 2020.
- Atefeh Mehrabi, **Aninda Manocha**, Benjamin C. Lee, Daniel J. Sorin."Bayesian Optimization for Efficient Accelerator Synthesis." In *ACM Transactions on Architecture and Code Optimization (TACO)*. ACM 2020.
- Opeoluwa Matthews, **Aninda Manocha**, Davide Giri, Marcelo Orenes Vera, Esin Tureci, Tyler Sorensen, Tae Jun Ham, Juan L. Aragón, Luca P. Carloni, and Margaret Martonosi. "MosaicSim: A Lightweight, Modular Simulator for Heterogeneous Systems." In *The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*. IEEE Press, 2020.
- Atefeh Mehrabi, **Aninda Manocha**, Benjamin C. Lee, and Daniel J. Sorin. "Prospector: Synthesizing Efficient Accelerators with Statistical Learning." In *Proceedings of the Design, Automation and Test in Europe Conference (DATE)*. IEEE Press, 2020.
- Atefeh Mehrabi, **Aninda Manocha**, Benjamin C. Lee, and Daniel J. Sorin. "Prospector: Synthesizing Efficient Accelerators with Statistical Learning." In *The Career Workshop for Women and Minorities in Computer Architecture (CWWMCA)*. 2019.

Work Experience

August 2022 – May 2022 | **Research Intern, NVIDIA, Austin, Texas [Virtual]**

- Characterized memory access patterns based on page reuse distances in irregular applications
- Designed a hardware mechanism to identify data worth backing with huge pages (2MB on x86) without requiring any OS overhead
- Developed a hardware-OS co-design to leverage the identification of huge page candidates in page size promotion decisions performed by the OS, and ultimately reduce address translation overheads for irregular applications

C++ | Huge Pages | Linux | OS | Python

August 2021 – May 2021 | **Research Intern, NVIDIA, Austin, Texas [Virtual]**

- Characterized the GPU memory capacity and bandwidth requirements of emerging workloads in the domains of graph analytics and machine learning
- Added GPU simulator support for aggressive memory-side next-line prefetching techniques
- Developed and evaluated a DRAM state-aware prefetching approach to improve the bandwidth efficiency and performance of next-generation GPU memory hierarchies

C++ | DRAM | GPUs | Prefetching | Python

August 2020 – May 2020 | Research Intern, Microsoft, Redmond, Washington [Virtual]
- Conducted an extensive literature survey on state-of-the-art techniques for page management and presented this survey to software, OS, and hardware experts working in this space
- Designed a hardware mechanism for page management in a system with disaggregated memory
- Created a software model of the mechanism to explore page management policies via simulation
- Developed an RTL prototype of the mechanism to demonstrate its feasibility and practicality

C++ | Disaggregated Memory | Page Management | Python | Verilog

August 2017 – May 2017 | Software Engineering Intern, Adobe, San Francisco, California
- Developed an intelligent thumbnailing algorithm that identified the most representative frame of several different marketing videos
- Integrated algorithm into the video processing workflow for dynamic media in Scene7 and Adobe Experience Manager to significantly reduce existing server overhead and improve software reliability
- Created a suite of tests that verified proper thumbnail generation and server communication

C++ | Java | Image and Video Processing | Maven | Perforce

August 2016 – May 2016 | Software Engineering Intern, Cisco Systems, San Jose, California
- Developed a suite of scripts to automate the testing and monitoring of various events, such as crash/traceback checks, hardware boots/failovers, configuration loss checks, and data collection
- Performed over 75 verifications and triggers (conditions to dictate routing and normalization logic) among Facebook, Google, Sprint, and Telstra profiles
- Created a web application to dynamically display quality metrics progression of routing platforms

Flask | MongoDB | Python | React | Tcl | Web Development

July 2014 – June 2014 | Software Engineering Intern, Lenovo, Morrisville, North Carolina
- Created various benchmarking scripts to be used as part of the System Integration Test (SIT) program
- Evaluated the performance of various servers before they are released to the enterprise server market
- Analyzed and compared several aspects of firmware and hardware of released and unreleased servers

Java | Python | Operating Systems

Leadership and Teaching

Present – June 2020 | Mentor, Duke Technology Scholars Program
- Mentored and mentoring three undergraduate female-identifying students as part of a mission to empower the next generation of diverse leaders who will increase innovation in the tech industry
- Guide mentees in evaluating short-term and long-term career decisions, setting goals and assessing progression towards them, and networking in both academic and industry settings
- Provide advice on how to navigate undergraduate research experiences, graduate school application processes, and industry internships

May 2018 – May 2017 | Treasurer, Wiring With Women
- Served as an executive board member of a student organization dedicated to supporting and providing a community for women in technology
- Assisted in the creation and organization of various events, including networking/recruiting, course selection advice, resume workshops, Lean-In circles, and general body meetings
- Managed all financial aspects of the organization

Spring 2018 – Spring 2017 | Teaching Assistant, Duke University
- ECE/CS 250: Computer Architecture (Spring 2018)
  - Instructor: Benjamin C. Lee
- CS 330: Design and Analysis of Algorithms (Spring 2018)
  - Instructor: Debmalya Panigrahi
- ECE/CS 250: Computer Architecture (Fall 2017)
  - Instructor: Tyler Bletsch
- ECE/CS 250: Computer Architecture (Spring 2017)
  - Instructor: Daniel J. Sorin

Projects

Automated Generation of Transactional Models for Formal Verification with SVA March 2020 - May 2020

A framework that can automatically generate models of RTL module interactions and their corresponding assumptions and assertions to ensure that liveness properties in a chip (or module) design are satisfied to guarantee forward progress.

Formal Verification | Python | SVA | Verilog

Cache Performance Improvement with Machine Learning March 2019 - May 2019

github.com/amanocha/mlcache

A system design that uses online and reinforcement learning techniques to predict ahead of time whether memory accesses will hit or miss in the cache. An average performance speedup of 2.93x is achieved with the use of lightweight classifiers.

Machine Learning | Python | scikit-learn

Superscalar RISC-V Processor October 2018 - January 2019

A two-wide superscalar in-order processor that can fetch and issue two instructions simultaneously. The processor can execute 43 instructions from the RISC-V ISA as well as various C benchmarks. This processor was also integrated into the OpenPiton framework.

Assembly | C | Verilog

Automatic Transmission System Verification March 2018 - May 2018

A timed automata representation of a 4-speed automatic transmission system that has four forward gears and one reverse gear. The constructed and verified model is paired with a simulation of the dynamic physical system.

Formal Verfication | Model Checking | UPPAAL | Simulink

Electric Keyboard November 2017 - December 2017

A 13-key piano built from 3D-printed keys and light sensing circuits and paired with graphics that display musical notes played in real time. The keyboard is controlled by digital logic and MIPS instructions that run on a custom pipelined processor that is deployed on an FPGA.

Assembly | Circuits | FPGA | ModelSim | SketchUp | Verilog

Voyij Lens January 2017 - April 2017

An Android application that uses augmented reality to guide users to various points of interest in Alaskan tourist cities through the phone's camera lens. This software was developed for Voyij, a cruise and travel app for day-to-day trip planning in Alaska.

Android | Augmented Reality | Mobile Development

Voogasalad December 2016

github.com/amanocha/voogasalad

A game authoring engine and environment that allows users to build a variety of 2D role-playing games using several available objects that have configurable attributes. Users can then save the games they create as well as play them.

Java | JavaFX | Object-Oriented Programming | XML

Foodpedia November 2016

HackDuke 2016 Submission github.com/amanocha/foodpedia

A web application that assists individuals in developing healthy relationships with food through personalized meal plans designed based on health information. An additional journaling feature allows users to document what they eat and represent their feelings with emojis.

Flask | HTML/CSS | JavaScript | Nutritionix | Photoshop | Python

Coursework

› Advanced Computer Networks • Advances in Automated Reasoning • **Computer Architecture** • Computer Vision • Cyberphysical Systems • Design and Analysis of Algorithms • **Digital Systems** • Engineering Software Maintainability • Fundamentals of Machine Learning • Image and Video Processing • Microelectronic Devices and Circuits • Operating Systems • Programming Languages • Robotics and Automation • Signals and Systems • Software Design and Implementation • Startup Software • **Systems and Machine Learning**

Skills

Programming	Assembly, Bash, **C/C++**, **Java**, Javascript, MATLAB, **Python**, **Verilog**
Frameworks	Express, Flask, Gem5, HTML/CSS, JQuery, LLVM, Node, PySpark, Simulink, Sniper
Design Tools	Altera Quartus, AutoCAD, ModelSim, PSPICE, **Vivado**
Development Tools	**Git**, Eclipse, IntelliJ Idea, Maven
Operating Systems	Android, **Linux**, **UNIX**

Awards and Honors

March 2020	NSF Graduate Research Fellowship Recipient
February 2020	ISPASS 2020 Best Paper Nomination
Fall 2015 - Spring 2018	Duke University Pratt School of Engineering Dean's List
December 2017	Duke Electrical and Computer Engineering Fall 2017 Independent Study First Place Poster
May 2017 - August 2017	Duke Technology Scholar
November 2016	HackDuke 2016 Novice Track Winner
May 2016	Duke STEAM (STEM + Art) Challenge 4th Place Winner
February 2015	Mathematical Contest in Modeling (MCM) Honorable Mention